

Application No. 10/730,002
Amendment dated May 2, 2006
Reply to Office Action of March 2, 2006

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1 – 13 (cancelled)

Claim 14 (currently amended) The domino logic circuit of claim [[13]] 19 wherein the first dynamic logic stage comprises two p-mosfet transistors driven by separate phases of the multi-phase clock.

Claim 15 (currently amended) The domino logic circuit of claim [[13]] 19 wherein the second dynamic logic stage comprises two n-mosfet transistors driven by separate phases of the multi-phase clock.

Claim 16 (currently amended) The domino logic circuit of claim [[13]] 19 wherein:
the first dynamic logic state performs any one of:
an OR-precharge function;
a domino-precharge function; and
the second dynamic logic stage performs any one of:
an AND-evaluate function;
an OR-evaluate function; and
a domino-evaluate function.

Claim 17 (currently amended) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:
a first dynamic logic stage comprising a precharge clock circuit comprising two p-mosfet transistors respectively driven by separate phases of the multi-phase clock;
a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock;
~~and The domino logic circuit as claimed in claim 14 comprising~~
dynamic gates directly coupled back-to-back at cell boundaries without an intervening static gate and the domino logic circuit performs a dynamic cascaded OR-precharge/domino-evaluate function.

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Claim 18 (currently amended) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:

a first dynamic logic stage comprising a precharge clock circuit comprising two p-mosfet transistors respectively driven by separate phases of the multi-phase clock;

a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock;
~~and The domino logic circuit as claimed in claim 14 comprising~~

dynamic gates directly coupled back-to-back at cell boundaries without an intervening static gate and the domino logic circuit performs a dynamic cascaded domino-precharge/AND-evaluate function.

Claim 19 (currently amended) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:

a first dynamic logic stage comprising a precharge clock circuit comprising at least one p-mosfet transistor respectively driven by a separate phase of the multi-phase clock;

a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock;
~~and The domino logic circuit as claimed in claim 13 further comprising~~

a secondary precharge network ~~[[.]]~~ comprising ~~[[.]]~~ at least one p-mosfet transistor respectively driven by the separate phase of the multi-phase clock.

Claim 20 (currently amended) A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:

a first dynamic logic stage comprising a precharge clock circuit comprising two p-mosfet transistors respectively driven by separate phases of the multi-phase clock;

a second dynamic logic stage comprising an evaluate clock logic circuit comprising at least one n-mosfet transistor respectively driven by a separate phase of the multi-phase clock;
~~and The domino logic circuit as claimed in claim 14 further comprising~~

a secondary precharge network ~~[[.]]~~ comprising ~~[[.]]~~ two p-mosfet transistors respectively driven by the separate phases of the multi-phase clock.